

Claims

[c1] 1. An integrated circuit package comprising:

- a semiconductor die of plural separate power supply voltage domains;
- a switch mode DC-to-DC converter including at least:

 - an inductor core and windings;
 - a power switching transistor; and
 - an output voltage fixing circuit.

[c2] 2. The integrated circuit package of claim 1 wherein said semiconductor die comprises a :

- voltage reference; coupled to an error amplifier; and a
- voltage comparator;
- for use in the feedback loop of the output voltage fixing circuit of said DC-to-DC converter.

[c3] 3. The integrated circuit of claim 2 wherein said semiconductor die comprises:

- a band-gap reference for a plurality of uses, buffered for one of such uses as the:
- voltage reference coupled to:

an error amplifier and
a comparator
for use in the feedback loop of said DC-to-DC con-
verter.

- [c4] 4. The integrated circuit of claim 1 wherein said semi-conductor die comprises a decoder that compares an entry from a table corresponding to the present power state of said semiconductor die to a clock counter frequency divider output to determine duty cycle and/or switching frequency of said power switching transistor for said output voltage fixing circuit.
- [c5] 5. The integrated circuit of claim 4 wherein said table of entries of clock counter values to determine duty cycle is encoded within logic within said semiconductor die.
- [c6] 6. The integrated circuit of claim 4 wherein said table of entries of clock counter values to determine duty cycle is contained within non-volatile memory.
- [c7] 7. The integrated circuit package of claim 1 wherein the power transistor gate-driving signal output from said semiconductor die is connected through a charge pump circuit to optimize efficiency of the power switching transistor of said DC-to-DC converter.
- [c8] 8. The integrated circuit package of claim 1 also com-

prising a substrate of fiberglass resin epoxy of type FR4 based laminate material for mounting said DC-to-DC converter components.

- [c9] 9. The integrated circuit package of claim 8 wherein said semiconductor die contains a plurality of pads from which to accept a binary number offset for fine tuning the duty cycle and/or switching frequency by modifying the value compared to the clock counter frequency divider in said output voltage fixing circuit of said DC-to-DC converter.
- [c10] 10. The output voltage fixing circuit of claim 9 wherein said binary number offset is embodied within fusible leads on the substrate that are electrically or mechanically trimmed or laser-trimmed at the factory.
- [c11] 11. The output voltage fixing circuit of claim 9 wherein said binary number offset is embodied within a wire-bonding option during assembly of said semiconductor die pads to the lead frame of said integrated circuit package.
- [c12] 12. The integrated circuit package of claim 8 wherein the power transistor gate driving signal output from said semiconductor die is connected through a trimmed delay circuit to fine tune the duty cycle of pulse width modula-

tor or pulse frequency modulator of the output voltage fixing circuit of said DC-to-DC converter.

- [c13] 13. The output voltage fixing circuit of claim 12 wherein said trimmed delay circuit further comprises a printed film resistor on the substrate that is laser-trimmed at the factory.
- [c14] 14. An integrated circuit package comprising:
 - a substrate of fiberglass resin epoxy of type FR4 based laminate material for mounting:
 - a semiconductor die of plural separate power supply voltage domains;
 - a switch mode DC-to-DC converter including at least
 - an inductor core and windings,
 - a power switching transistor, and
 - an output voltage fixing circuit.
- [c15] 15. The output voltage fixing circuit of claim 9 wherein said binary number offset is embodied within a wire-bonding option during assembly of said semiconductor die pads to said substrate of claim 14.
- [c16] 16. A method for design and fabrication of an integrated circuit package comprising a semiconductor die of plural separate power supply voltage domains with an inte-

grated switch mode power supply, said method comprising steps of:

designing a semi-custom or standard cell library based digital core and obtaining from the design automation tools power consumption estimates in various power states given known clocking rates;

determining switch mode power supply frequency, inductance, and duty cycles for various power states given the above power consumption estimates and system clocking;

fabricating said semiconductor die for prototyping purposes, packaged without said integrated switch mode power supply;

characterizing said prototype semiconductor die for power consumption over all operating power states and environmental conditions and process variations;

fabricating said switch mode power supply onto final production substrates;

trimming the output voltage fixing circuit of said switch mode power supply after a probe test to determine the output voltages at given duty cycles versus output currents defined by the known characterization data;

bonding and molding or sealing with epoxy said semiconductor die and power supply substrate into an integrated package.

- [c17] 17. The method of claim 16 wherein said step of trimming the output voltage fixing circuit comprises a further step of binning said final production power supply substrates into the appropriate wire-bonding assembly line to set the proper binary number offset of the output voltage fixing circuit.
- [c18] 18. The method of claim 16 wherein said step of trimming the output voltage fixing circuit comprises a further step of breaking fusible leads on said final production power supply substrate to set the binary number offset of the output voltage fixing circuit.
- [c19] 19. The method of claim 16 wherein said step of trimming the output voltage fixing circuit comprises a further step of laser trimming a printed film resistor forming a delay circuit of the output voltage fixing circuit on said final power supply substrate.
- [c20] 20. The method of claim 16 wherein said step of trimming the output voltage fixing circuit comprises a further step of programming a non-volatile memory with entries of clock counter values to determine duty cycle and/or switching frequency corresponding to each power state of the semiconductor die.
- [c21] 21. A method for design and fabrication of an integrated

circuit package comprising a semiconductor die of plural separate power supply voltage domains with an integrated switch mode power supply, said method comprising steps of:

- designing a semi-custom or standard cell library based digital core and obtaining from the design automation tools power consumption estimates in various power states given known clocking rates;
- determining switch mode power supply frequency, inductance, and duty cycles for various power states given above power consumption estimates and system clocking;
- fabricating said semiconductor die for prototyping purposes, packaged without said integrated switch mode power supply;
- characterizing said prototype semiconductor die for power consumption over all operating power states and environmental conditions and process variations;
- fabricating said switch mode power supply onto final production substrates;
- bonding and molding or sealing with epoxy said semiconductor die and assembled final power supply substrate into an integrated package.